Low frequency noise characterization and modeling of microwave bipolar devices : application to the design of low phase noise oscillator

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Abstract — **This paper addresses advanced low frequency noise measurements and modeling of SiGe HBTs. Results have been implemented into a non linear Gummel Poon model which has been validated through the design of a DRO made of an integrated SiGe negative resistance in the 10 GHz range. We have obtained phase noise of -105 dBc/Hz at 10 kHz offset, which is close to the state of the art, and we have demonstrated a design technique that provides an accurate phase noise prediction.**

I. INTRODUCTION

The future wireless communications and space applications will have to feature ultimate performance in term of quality of service. For instance, it is understood that the systems will have to work "any time" "anywhere" that needs some enhanced performance concerning the different electronic modules within the system. Among the different specifications to be considered, one is gaining more and more importance and is related to the stability of the microwave and the millimeter wave source modules. Today, there is no generic method to design a low phase noise oscillator. Usually people use their home made "know how" and the low phase noise character is only achieved through some prototype that is difficult to reproduce for an industrial implementation. It is furthermore well known that low frequency (LF) noise sources within the active device drive the phase noise behavior of the microwave oscillator through the up-conversion processes. Today the non linear methods used to calculate phase fluctuations have been enhanced and they give reasonable results. The main issue is now related to the LF noise sources modeling and, more important, to their physical features.

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The conventional approach involving input or output equivalent noise generators do not provide accurate results. It is therefore necessary to work towards the development of a generic method that allows to build a low frequency noise model involving intrinsic noise sources with a larger physical meaning. The other important issue deals with the fact that the model must be compatible with a standard CAD platform. In this paper, we report on a generic technique allowing to develop a low frequency noise model of a SiGe HBT and this model will be used for the design of a low phase noise semi-integrated oscillator in the X band range.

The paper is organized as follows : section II presents a brief overview of the SiGe technology for the devices under discussion. In section III, we carry out a complete low frequency noise characterization of SiGe HBTs from STMicroelectronics. The intrinsic low frequency noise model derives from the correlation resistance properties as it will be outlined in the paper. The model has been introduced within a non linear Gummel Poon model modified in order to take into account the intrinsic noise sources. Section IV focuses on the design of a negative integrated resistance, using the advanced non linear noise model, that has been associated with an off-chip dielectric resonator in order to realize a very low phase noise oscillator. In the last section, we present a comparison between the measured and simulated oscillator phase noise.

II. TECHNOLGY

The different investigated SiGe HBTs devices have been processed through a SiGe HBT BiCMOS technology currently in commercial production (STMicroelectronics BiCMOS6G). Details on the process can be found in [1].

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The investigated devices feature three emitter fingers of 0.4 µm by 20 µm. In order to minimize the low frequency noise, we have considered different topologies made of two transistors in parallel (the total area emitter is therefore A_E=48 µm²), three transistors in parallel (the total area is then A_E=72 µm²), and four transistors in parallel (total area of A_E=96 µm²).

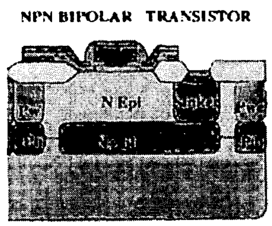

Fig. 1 Schematic cross-section of the BiCMOS6G HBT[1].

A schematic HBT cross-section is shown in Figure 1. Major electrical specifications of a typical device are summarized in Table 1.

β (current gain)	BV_{CEO} min.	peak f_T	peak f_{max}
100	3.6 V	45 GHz	60 GHz

Table 1 Electrical parameters for a typical SiGe HBT.

III. LFN Results

A. LFN Measurement

In order to accurately characterize the LF noise, a dedicated test set has been implemented [2]. It consists in two low noise transimpedance amplifiers that provide the base and collector current noise sources (referred to respectively as S_{IB} and S_{IC}) and the cross spectrum between this two noise sources (referred to as S_{IBIC^*}) [2]. In order to develop a non linear model, noise measurements have been performed for a collector current density ranging from 4.6 to 23 kA/cm², and for a collector emitter voltage ranging from V_{CE}=0.5 to 1.5 V. Fig. 2 depicts the S_{IB} evolution versus frequency. The spectrum exhibits a 1/f noise dependence at low frequency followed by a plateau in the 10 kHz range. This plateau magnitude is expected to be equal to $2qI_B$ [2]. We can see in Fig. 2 that the plateau magnitude is above the shot noise level. A similar behavior has been found at all bias conditions, and for all the devices that have been measured, meaning that the difference is related to an additional noise source. We furthermore have observed that the difference between the measured noise at high frequency and the shot noise magnitude scales as I_B^2. From these assumptions, it is suggested that this excess noise could be related to a generation recombination noise source featuring a cut off frequency in the1MHz range. To clarify this point, it would be interesting to perform low temperature noise measurements in order to confirm or not our expectation. Concerning the noise evolution versus the collector emitter voltage, it has been observed that both S_{IB}, S_{IC} and S_{IBIC^*} spectra are all independent from V_{CE}.

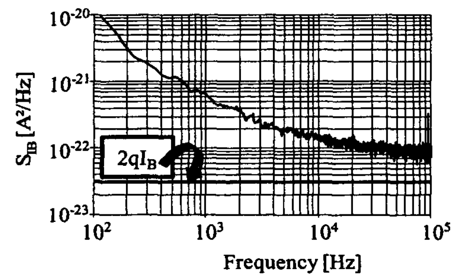

Fig. 2 Comparison of S_{IB} and $2qI_B$ (J_C=23 kA/cm², V_{CE}=1V, A_E=48 µm²).

B. LFN Model

The low frequency noise model has been developed using an original method based on the correlation resistance concept (deriving from the correlation between the noise generators). This method compares the value of the correlation resistance with the addition of the base and emitter resistances [3]. From such a comparison, it is possible to identify the excess noise sources that must be considered within the device. More details concerning the method will be given at the conference. It has been found that the HBTs under discussion here feature six intrinsic noise sources as shown in Fig. 3 :

- e_{rb} and e_{re} for noise in the emitter and base resistance,
- i_{be2} for the emitter-base junction,
- i_{ce} at the collector emitter terminal,
- i_{bc} and i_{be1} for surface noise sources.

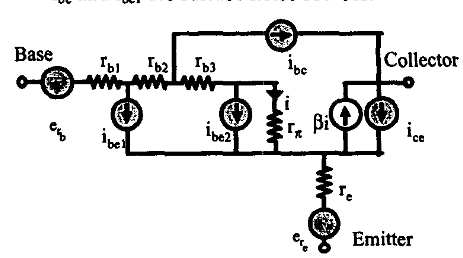

Fig. 3 LF noise model of the investigated SiGe HBT.

This model provides a good agreement between theoretical and experimental data. The intrinsic noise sources have been implemented into a non linear Gummel Poon model in order to get an accurate description of the phase noise of a microwave oscillator.

IV. Oscillator

In order to validate our approach, we have designed a low phase noise monolithic negative resistance to be further associated with a dielectric resonator at 10.3 GHz.

A. Negative resistance design

We have chosen a series feedback topology in order to design the oscillator since it has already been reported that such a topology represents the best trade-off between high gain and low phase noise [4]. The negative resistance is obtained through a capacitor C_E placed on the emitter terminal. Fig. 4 represents the topology of the negative resistance. The active device features an emitter area of A_E=48 µm² in order to have enough gain at 10 GHz.

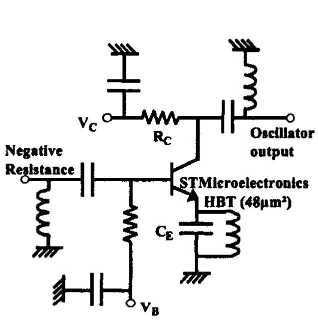

Fig. 4 Negative resistance topology.

The negative resistance layout is shown in Fig. 5. Dimensions of this circuit are 0.83*0.83 mm². It has been processed by STMicroelectronics using the integrated circuit BiCMOS6G technology featuring 5 metal levels.

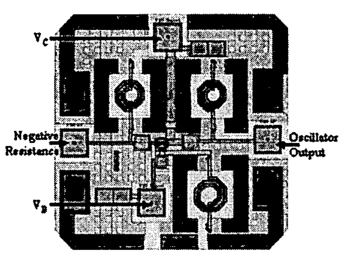

Fig. 5 Negative resistance layout.

We display, in Fig. 6, the negative resistance S_{11} measured either on wafer or on the packaged device (S_{11}'s of 10 dB and 6.2 dB are respectively observed at 10 GHz). The difference between these two measurements is attributed to the bonding wires used in the package.

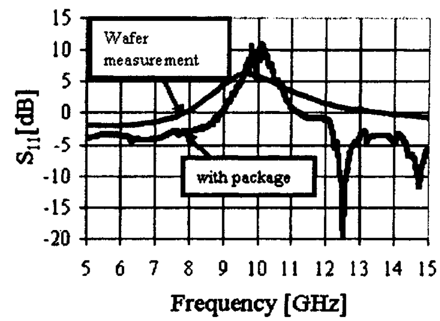

Fig. 6 S_{11} measurements of the negative resistance either on wafer or packaged.

B. DRO

The dielectric Murata resonator, that has been used with the negative resistance, features an unloaded Q of 35000. The assembly has been realized on a Teflon substrate (loss tangent tan δ=0.0035, relative permittivity ε_r=9.5). Copper lines are used as interconnects. A photograph of the DRO is given in Fig. 7. The dielectric resonator loaded quality coefficient was measured to be about 2000 and its transmission was -5 dB.

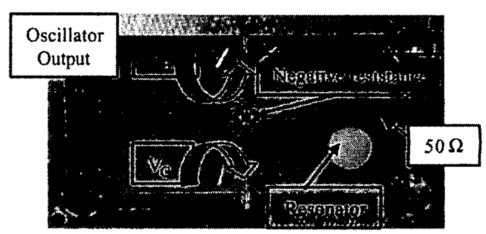

Fig. 7 Photography of the DRO at 10.3 GHz including the negative resistance IC and the dielectric resonator.

The DRO works as expected : the oscillation frequency is 10.3 GHz, the output power is 0 dBm and the power consumption is 35 mW. Next section addresses phase noise data.

III. Phase-Noise Results

A. Phase noise measurement

The noise set-up uses a passive method involving cross-correlation technique [5]-[6]. A minimization technique of the amplitude modulation noise is also used. More details on the measurement technique can be found in [7].

Fig. 8 compares the measured and predicted phase noise versus the offset frequency from 10 Hz to 100 kHz.

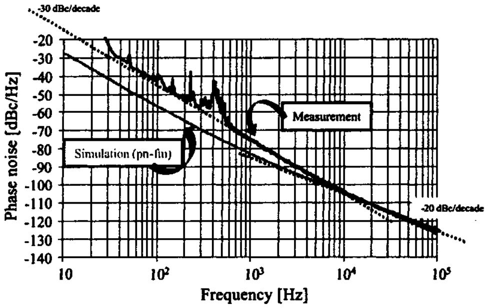

Fig. 8 DRO 10.3 GHz phase noise measured and simulated versus the offset frequency.

The spectrum disruptions around 400 Hz are the consequence of the electrical supply harmonics and/or microphonics noise. The measured spectrum shows a phase noise of –105 dBc/Hz at 10 kHz off the carrier. This result is not only very close to the state of the art but it has also been obtained using a MMIC die.

B. Phase noise simulation and comparisons

Concerning the phase noise simulation, we used the modified non linear model (involving the LF noise sources) and the pushing technique available in a commercial microwave software [8]. The simulated spectrum in Fig. 8 shows, as expected, a -30 dB/decade slope for the 1/f noise converted into phase noise and also a –20 dB/decade one for the up-converted thermal and shot noise.

We observe an excellent agreement between measured and simulated phase noise in the –20 dB region : the same phase noise as predicted (–125 dBc/Hz) is measured at 100 kHz off carrier. Concerning the 1/f noise description (–30 dB region), the agreement is less satisfactory meaning that further investigations are needed in order to investigate more deeply the physical location of the different 1/f noise sources and to built a more accurate non linear noise model. Nevertheless, present results have been compared with a conventional SPICE approach and they improve the accuracy of the phase noise simulation by up to 20 dB.

V. Conclusion

From an exhaustive low frequency noise characterization, we have developed an intrinsic non linear SiGe HBT low frequency noise model. In order to validate this model, we have demonstrated a very low phase noise X-band DRO involving an integrated negative resistance realized with a BiCMOS SiGe process. The 10.3 GHz phase noise has been found to be –105 dBc/Hz at 10 kHz off the carrier which is a very relevant performance for an IC. The advanced low frequency noise model has been implemented into a commercial microwave software and we have obtained a satisfactorily agreement between predictions and measurements demonstrating that an accurate low frequency noise characterization and modeling is needed for an accurate phase noise description. We also have to emphasize that the modeling technique proposed in this paper could also be used for other microwave devices.

Acknowledgement

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